Low Cost T/R Modules for Planar Arrays

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Abstract

For phased arrays to be viable in present and future radar systems, T/R module designs will need to be lower cost, lighter weight, and more producible. The T/R module presented in this paper provides a new approach for both module and array design. A planar approach is presented in which individual T/R modules are 'plugged' into the array allowing for easy maintenance of the array.

Introduction

The challenge of this effort was to design, develop, and test a low cost T/R module that would support a planar array architecture. While traditional T/R modules (brick or slat approach) construct the module in the plane perpendicular to the array face [1], the approach presented here constructs the module in the plane parallel to the array or 'coplanar' to the array face [2,3], while still using standard 'chip and wire assembly processes. A number of issues needed to be resolved during the design to enable this coplanar module approach. The package needed to support a perpendicular RF interconnect, three dimensional RF routing and a low profile interconnect between multiple packages. In addition, a MMIC chip set was needed that required minimal area, allowing the module to fit in the array grid spacing. Figure 1 shows the T/R module that was constructed and tested while addressing these design issues.

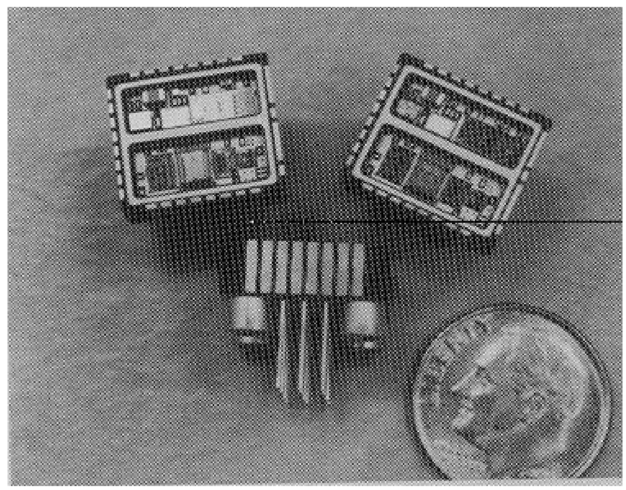

Figure 1. Planar Array T/R Module Showing RF Assembly.

The block diagram for the T/R module was developed such that the transmit and receive functions could share as many functions as possible (phase shifter, attenuator, and predriver/post amp). Figure 2 shows the block diagram for the planar array module. As seen in Figure 1 the present T/R module contains four GaAs MMICs. One additional aspect of this architecture is that it supports further levels of chip integration, with the next step being only three GaAs MMICs (LNA/Power amp/control MMIC). One additional advantage of this approach is the 'common' amplifier stages which remain on (i.e. in CW mode) and are therefore thermally stable.

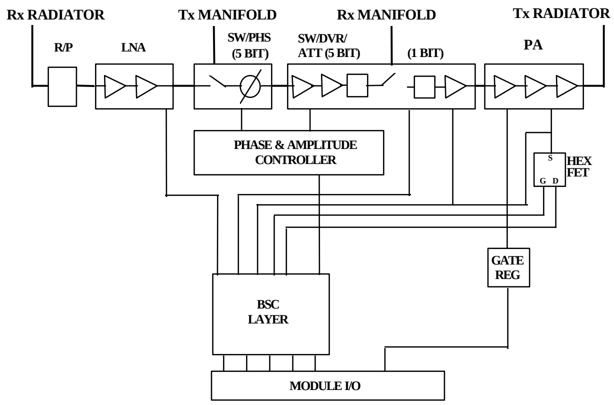

Figure 2. T/R Module Block Diagram.

There are a number of advantages to this T/R module approach. The ease of assembly into the array is greatly enhanced through the use of pins and connectors for all interconnects, the module is simply plugged in during array assembly. The Ease of assembly into the array also allows for easy removal from the array for maintenance and repair. The low profile of the T/R module significantly reduces the space required for the modules in the array, thus greatly reducing the weight of the system. The ease of removal allows for the possibility that the modules could be tested in the array environment rather than individually after assembly. Assembly of the T/R module uses existing 'chip and wire' processes and is therefore easily produced and low risk. Cost has been addressed with fewer and smaller MMICs than most existing T/R modules with only two substrate/housings being needed. The total area for the MMIC chip set was only 27.7 mm^2 relative to a 5 watt power amp. No special substrate material was required, a standard commercial multilayer high temperature cofired ceramic (HTCC) was used.

Design Approach

The first issue to be addressed was to develop a chip set to support the module architecture, but was also of minimal area and risk. The size of the MMICs was important, not only for cost, but also, to maintain a single RF layer, as the module needed to fit within the allotted element spacing. The LNA is a commercially available Litton LMA 219B, providing excellent noise figure. The 5 bit phase shifter/switch MMIC is simply a modification of an existing Northrop Grumman ESSD MIMIC phase shifter design in which a switch was added. The attenuator/switch/driver amp is the integration of an existing attenuator design with a switch and three gain stages. Two of the gain stages serve as both post amp and predriver, allowing for CW operation. The third gain stage serves as the driver amp which is pulsed. The output power (and complexity) of the driver stage is minimized by making the power amp a three (gain) stage MMIC. The power amp as stated is a three stage device based on an existing two stage MMIC currently in production for the Northrop Grumman Modar airborne weather radar. The approach for MMIC development was to minimize the risk undertaken with their development by either using existing MMICs or making minor modifications to existing MMICs.

The packaging approach was probably the most challenging aspect in the design of the module. Some of its attributes include the need for orthogonal RF interconnects, three dimensional RF routing, and low profile DC/logic interconnects between packages. Figure 3 shows views of the two unpopulated substrates of the T/R module. The array interface for the T/R module is on the bottom side of the RF substrate, containing all the array (DC/logic and RF) interconnects. A low cost solution for the orthogonal RF interconnects was developed by use of existing brazing techniques at the HTCC vendor. The shroud and center pin of the connector are separately machined and then brazed onto the substrate, the cost of each RF connector was under $ 3.00. The approach taken for the DC/logic interconnect between the substrates was that of a leadless chip

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carrier in which the two substrates are connected by soldering the side I/O of the two packages. One additional advantage of using multilayer ceramic is that the RF package could be 'channelized' (i.e. contain cavities below waveguide cutoff) at virtually no additional cost. This attribute greatly reduces the chance of any cavity or waveguide modes being present within the package, which may cause module instability.

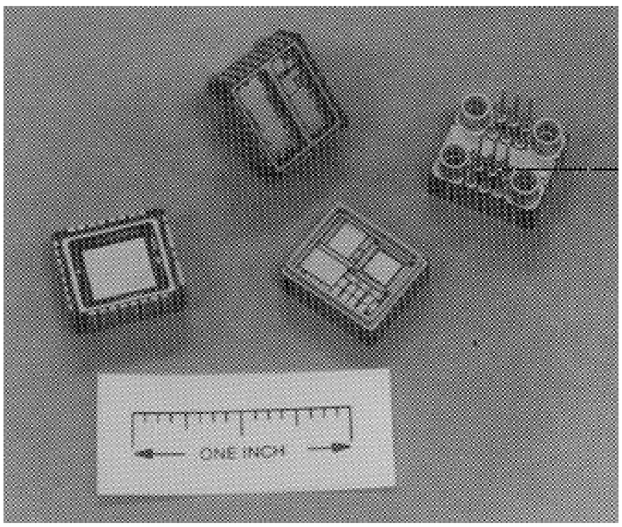

Figure 3. Unpopulated T/R Module Packages.

A number of RF transitions within the RF substrate required modeling using HFSS due to their 3-dimensional nature. The primary challenge in the modeling/design of the RF package was the RF connector/substrate interface. The diameter of the braze pad for the center pin of the RF connector was the limiting factor in the bandwidth of the package, this pad presented a large shunt capacitive affect, relative to the ground pad provided for the connector shroud. Figure 4 Shows the modeled match for both the 'raw' untuned interface and the final 'tuned' interface. Greater bandwidth could be obtained with smaller diameter braze pads for the center pin. Other structures that were modeled included stripline to stripline and stripline to MMIC transitions. Return Losses for the stripline to stripline transitions were modeled at better than -20 dB and the stripline to MMIC transition was modeled at better than -20 dB over most of the band rolling off to approximately -17 dB at the upper edge of the band due to bond wire inductance.

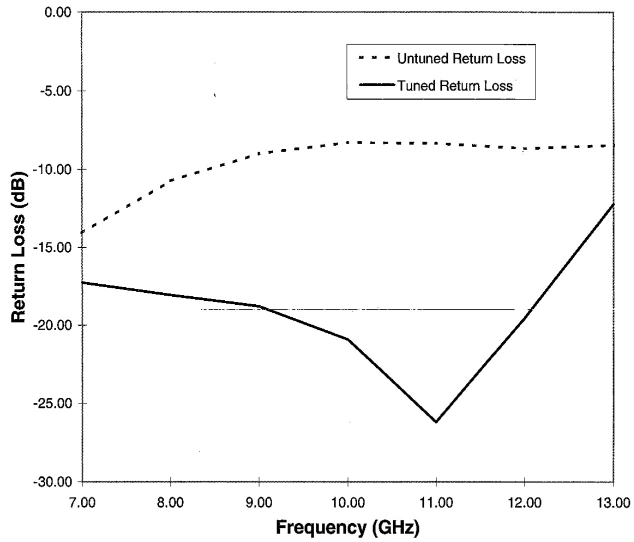

Figure 4. Modeled Results for the Connector Package Interface.

Silicon power and control functions included a module controller for control of the phase shifter, attenuator and T/R switches within the module. In addition, voltage regulation was provided on the module for both transmit and receive. Only two regulators are used, one for the transmit gate, and the other for the drain bias on all the MMIC amplifiers. In addition, the drain bias regulator is used to control the high current switch (HEXFET) for the power amplifier.

The T/R module was fabricated in the ESSD automated module assembly and test facility, manufacturing design guidelines were followed to ensure ease of assembly. Results are show for first iteration devices of both GaAs and Si, in addition to the first iteration package.

The transmit the power for the complete T/R module is shown in Figure 5. For comparison, Figure 5 shows the output power both with and without the lid. The output power remains greater than 4 watts over the design band. In addition, as can be seen, there is no higher order ripple in the passband which would be indicative of feedback within the module, an indication that the cavities, or channels within the module greatly reduce feedback.

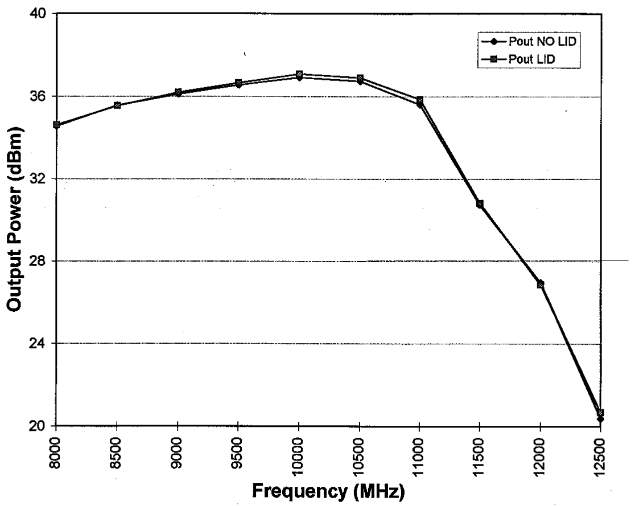

Figure 5. Measured Transmit Output Power With and Without the Lid.

The receive chain was tested with results for the gain and noise figure shown in Figure 6. The gain of the chain met the goal of greater than 20 dB over the band of interest. The rolloff in gain was due mainly to rolloff in the MMICs and higher than expected insertion loss in the substrate. The low order ripple (approximately one cycle) is primarily due to one of the bits in the attenuator and is being addressed in the next iteration of the MMIC. The noise figure only met the goal of less than 3 dB over a limited portion of the band, due to both higher than expected insertion loss in the substrate and a worse than expected match at the connector interface. Both these issues expect to be resolved in future iterations, through the use of lower loss 'white' HTCC and a smaller diameter braze pad for the RF pin.

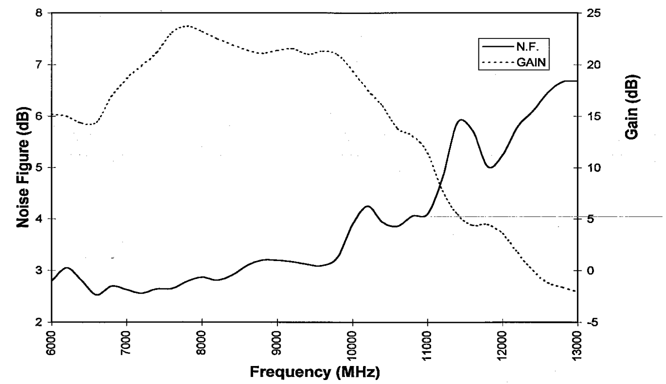

Figure 6. Measured Gain and Noise Figure of the Receive Chain.

Conclusion

The ability to design and fabricate producible modules for planar arrays has been demonstrated through the use of innovative packaging approaches. Excellent RF results have been demonstrated through the use of channelized RF cavities, which comes virtually free with the multilayer ceramic approach. While cost has been reduced over existing modules through increased integration, (i.e. fewer parts than existing modules) continued work is being performed to further lower the cost.

References

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